Performance Evaluation of a Communication Network for Digital Substation Automation System

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***Abstract*— Communications Network and Intelligent Electronic Devices (IEDs) are important functions of a substation automation system (SAS). Measuring the propagation delays and assessing the interoperability performance of IED's in an Ethernet architecture play a critical role in the operation of substation. This paper studies the application of Ethernet in Digital Substation Automation System (DSAS). Then several causes that greatly affect the performance of network are evaluated based on detailed test data. The results of such analysis proposed the key points of promoting a network in digital substation automation system**

***Keywords* Digital Substation, Automation, IEC61850, Network Performance, Ethernet, Media Accesses, Controller (EMAC)**

1. Introduction

With the development of computer embedded technology and network technology, substation automation system (SAS) has entered the phase of digital substation Automation System (DSAS), IEC61850 has become the only international standard of SAS based on Ethernet Network. It suggests that the standard Ethernet Network communication should be applied in DSAS as a communication method between IEDs from process level over bay level up to station level to guarantee data translation with high speed and reliability ultimately. Therefore, the performance of Ethernet Network has a great effect on efficiency and reliability of DSAS.

2. Digital Substation Automation System

Digital Substation Automation System makes substation as the research object, uses unified models to describe the digital information of substation, visualizes the physical devices, makes use of standard network communication platforms and realizes the information. Sharing and devices inter-operations DSAS will be the next phase of SAS development. The architecture of DSAS is divided into three levels, which are station level, bay level, and process level, Figure.1.shows Interface model of a substation automation system. IEC61850 suggests that the

Standard Ethernet Communication should be applied in substation automation system as the communication method between IEDs from process level (data acquisition, sensors, and actuators) over bay level (protection, monitoring and control task) up to station level. Ethernet Communication has become the character of DSAS.

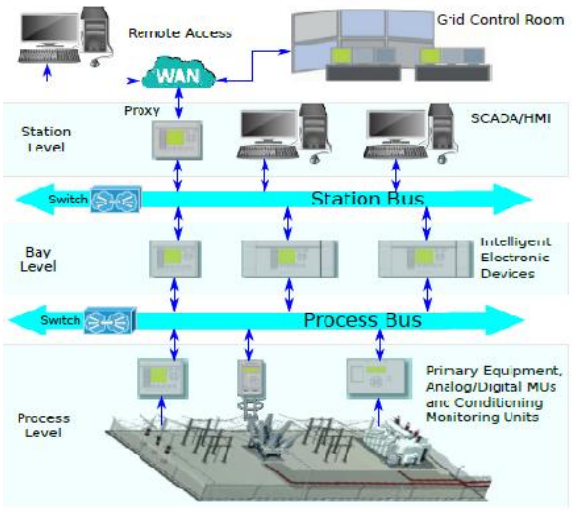

Figure.1 Shows Interface model of a substation automation system

Factors Affecting the Performance of a Network There are two kinds of factors that affect the network performance. They are hardware factors and software factors. Hardware factors include Ethernet Media Access Controller (EMAC)'s parameters (working mode, speed, FIFO depth, Jumbo Packet Support, Hardware Checksum Support and DRE Support, etc.,), PHY setting CPU processing speed, and other factors in the network transmission. Software factors mainly include an embedded real-time operating system and the driver of EMAC.

3.0 EMAC's mode

POLL. FIFO and DMA are three modes of EMAC. POLL mode is a scan mode whose efficiency is very low. It is often used to test EMAC.FIFO and DMA are an interrupt mode and mainly used to transmit/receive date.

FIFO MODE is a simple transmit and receive mode in EMAC, There are two channels, send channel and receive channel. Each channel has its own separate FIFO. Transmit starts when transmit data is put into FIFO first. Transmit complete interrupt will be generated by the EMAC after one transmit is completed successfully. As EMAC detects a packet is being received, EMAC will store received data into receive FIFO. Following the completion of successful receive, EMAC will generate a receive interrupt that means

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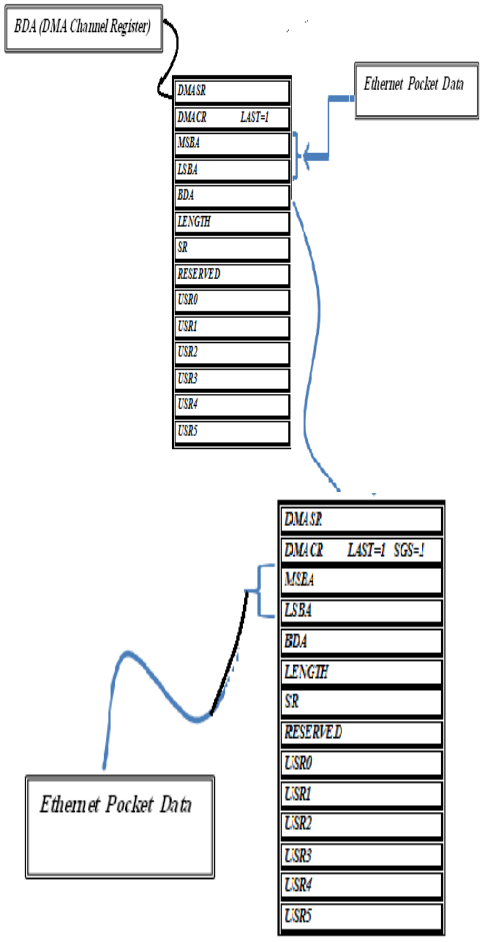
one receive is completed, However if an error occurs during The reception or if the receive packet FIFO becomes full and overruns, the EMAC will discontinue data storage into the receive packet and flush all the packet data stored there associated with the bad packet.

DMA MODE, DMA is a hardware mechanism that allows peripheral components to transfer their I/O data directly to and from main memory without the need for the system processor to be involved in the transfer. Use of this mechanism can greatly increase throughput to and from a device, because a great deal of computational overhead is eliminated. The buffer of descriptor (BD) provides a fixed length buffer to contain and access data. A buffer descriptor is as shown in figure2 DMA can be divided into three types, simple DMA, simple Scatter Gather (SG), DMA and Transmit/Receive Packet Scatter Gather DMA is mostly used and the most efficient one, The DMA mode that discussed in the paper is Transmit/Receive Packet Scatter Gather DMA



Figure,2. Buffer Descriptors List's structure.

Comparison between DMA and FIFO mode.

In theory, the performance of EMAC with DMA mode is better than with FIFO mode, but it is not absolute in the practical test, The reason is that DMA mode is more complicated than FIFO mode. So the EMAC driver mode needs a code to realize DMA function that means more time. in general, the performance of EMAC with FIFO mode is better when CPU speed is relatively low.

3.1 EMAC other Parameters

a) EMAC speed.

The faster EMAC, the better network performance. The ideal EMAC is Gigabit EMAC which supports full-duplex. This is the chief promote network performance.

b) FIFO Depth.

Designs a serial of hardware buffers to store transmitted/received data. The big FIFO depth will help for storing more data, reducing net frames discarding and promoting network transmit efficiency. At the same time, big FIFO depth guarantees EMAC can receive Jumbo Frame.

c) Jumbo Frame Support.

With this the EMAC can receive and transmit the frame whose data field size is bigger than 1500 bytes. The normal Ethernet frame size changes from 64 bytes to 1518 bytes, and the size of data field size changes from 46 bytes to 1500 bytes. This means that there is a fixed 18 bytes other fields even if data field of the frame is 46 bytes. So the bigger size of data frame, the better network performance.

d) Hardware Checksum and DRE Support.

- ***Hardware Checksum*** is the function that EMAC hardware completes computing Checksum field of Ethernet frame. This will reduce the time of creating Ethernet frame creating and speed up the Ethernet frame transmission**.**

- ***Data Realignment Engineer (DRE)*** allows unaligned source and destination addresses originating from the DMA controller [1]. When DMA works, memories alignment of buffer descriptors and data buffer is very important, especially in high speed transmission . The reason the time of dealing aligned is less than unaligned data, Many EMACs have strict demands on data alignment. For example, xilinx PLB_TEMAC IP demands data on 62-bit word boundaries [1]. But protocol software cannot guarantee by EMAC hardware or Ethernet driver. DRE is a mechanism to guarantee that the data alignment must be guaranteed, if there is there no DRE, software should copy the data to aligned memory to guarantee the data alignment. This will increase CPU time greatly.

3.2 PHY

Chip also have an effect on network performance. It is jumbo Frame Support of PHY. As shown in Table1 shown, there is a great difference in network performance between enable and disable Jumbo Frame Support of PHY.

3.3 CPU Performance

In order to get the application data segment, CPU must analyze the frame according to the protocol. Therefore, CPU speed will affect network performance greatly.

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3.4 Operating System and EMAC Driver

When hardware is same, the actual network performance depends on the EMAC driver. In EMAC driver design, designers should illuminate unnecessary operations, such as memory copy. In the EMAC driver, data buffer and the memory space of Buffer Descriptor used by EMAC DMA, mechanism should not be set cashable if can. Otherwise, it will bring up cache coherence problem that will make for transmitting and receiving error Ethernet packet and low network performance [2] Linux and VxWorks are two embedded RTOS used mostly in SAS IEDs. Different OS has different drivers

1) Linux EMAC Driver

- **Cash Coherence**

In Linux, DMA buffer allocation is called DMA mapping, There are two types of DMA mapping , consistent DMA mapping and streaming DMA mapping, depending on how long the DMA buffer is expected to stay around [2]. In Linux EMAC Driver consistent DMA mapping is used to locate DMA buffer descriptor space memories by calling consistent_alloc(), while streaming DMA mapping is used to allocate DMA data buffer space memories by calling pci_map_single(),consistent_alloc() allocates consistent pages and maps them to kernel;s vmalloc space< these pages are unique non-cashable pages. Pci_map_single() can also guarantee that the pages allocated are cache coherent. Hence there is not cache coherence problems in DMA memory allocating in Linux Driver.

2) VxWorks EMAC Driver

- **Cache Coherence**

Cache flash() and cacheInalidDate() are the function to flash and invalidate cache buffer in VxWorks. Cache coherence will be guaranteed by calling them in VxWorks drivers. The other to make driver more effectively is using cache-safe buffer allocation and cache flash/invalidate operation at the same time. You can use cacheDmaMalloc() to allocate Cache safe buffer, while use Cache_DMA_FLASH and

CACHE_DMA_INVALIDATE Macros to guarantee cache coherence, use CACHE_DMA_VIRT_TO_PHYS and **CACHE_DMA_PHYS_TO_VIRT** macros to convert between visual address and physical address. However, cache coherence must be guaranteed by calling flush/invalidate operation whatever method used. It needs software to realize this function. And it is very difficult to make sure that where the flush/invalidate codes should be added in EMAC driver . If the codes are added into wrong position, the performance of EMAC driver will be discussed greatly.

- **ZBUF**

VxWorks includes an alternative set of socket call based on a data abstraction called a ***zbuf,*** which permits you to share data buffers (or portion of data buffers) between separate modules. The **zbuf** socket interface allows applications to read and

write UNIX BSD sockets without copying data between application buffers and network buffers. The buffer copy and checksum computing are the most time-cost in the network protocol. ZBUF can reduce the time-cost data copy between buffers effectively. So the ZBUF socket can be used to save limited time resource and promote the real time ability of the system.

4.0 Tests and Evolution

The following tests all make to use of the netperf test bench program.

4.1 The Impact of Hardware on Network Performance

In this test, the development board is Xilinx ML405 whose key chip is a Xilinx V4 FPGA which combines PowerPC 405. The working frequency is 300 MHZ. The EMAC is Xilinx PLB-TEMAC IP core used as a net client while the development board is net server. TCPis the test protocol. The frame size of test data is 8,000 bytes. Test results are tabulated below in table1 whose working mode is SG-DMA. PHY chip is MARVELL88E111. VxWorks 6.4 is used as an operating system. The EtherNet physical connection is RJ45 cable. PC is as net client while the development board is a net server. TCP is the test protocol .

Jumbo size (byte)	ZBUF	H.W Checksum	PHY enable Jumbo Support	Performance (mbit/s)
9000	enable	enable	enable	545 **
9000	disable	disable	disable	218
1500	enable	enable	enable	309 **
1500	disable	enable	enable	157
9000	enable	disable	enable	358 **
9000	enable	disable	enable	361 **
9000	enable	enable	disable	190

** **Better Network Performance**

Table.1 Indicates the impact of hardware factors on network performance

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4.2 The Impact of Software on Network Performance

This test makes use of the development board designed and made by NARI Corp. R&D Center. The key chip of board is a Xilinx V2Pro7 FPGA, which combines PowerPC 405 and FPGA fabric into one integrated circuit [4]. The working frequency is 300 MHZ. In software, VxWorks 6.4 and Montavista Linux 3.1 are used as operating system separately. The Ethernet physical connection is fiber. PC is used as a net server, while the development board is a client. TCP is a test protocol and Test data's frame size is 8,000 bytes.

5.0 Ethernet Architectures modeled in OPNET

An optimized network engineering tool (OPNET) simulates a star architecture model of a typical 33/11kV substation whose single line diagram (SLD) is shown in Figure2. For simulation, LAN speeds of 10Mb/s and 100Mb/s

OS	ZBUF Support	Jumbo Size support	Cache Cohere 0n0ce	Performance(mbit/s)
Montavista Linux 3.3		**8982**	**OS Guarantee**	**200**
Vxworks 6,4	**Enable**	**9000**	**Driver Guarantee**	**110**
Vxworks 6.4	**Enable**	**9000**	**Driver not Guarantee**	**35**

Table2 indicates that the impact of Software factors on network performance

are considered. SAS exhibiting priority orders of different types of messages are listed in Table3. serving different IEDs within a digital substation.

Sr. No	Message Type	Priority	Byte size
1	Trip	5	50
2	Interlock	3	150
3	Status indication	2	200
4	Sample Value	4	98
5	File Setting	1	1000

Table3. Criticality of messages and its acceptable byte sizes.

All time critical messages, i.e., trip-1 type messages and interlocks, are trip-2 type messages etc. are assigned priority in descending order [5]. Figure. 3 shows two individual process bus in a star topology which are connected to router 1. These buses are designated A1 and A5 respectively as shown in Figure3 of the SLD and are isolated by 22kV bus tie circuit breaker. Figure.3, further exhibits an OPNET

model having various nodes and buses connected in star topology architecture via switch 1

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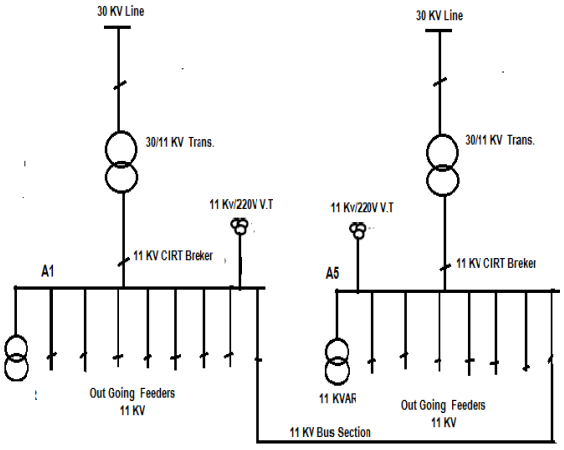

Figure.2 Shows Single line diagram of the 33/11-zone substation

Simulation results having LAN speed of 10 Mb/s is exhibited in figure.4 and 5

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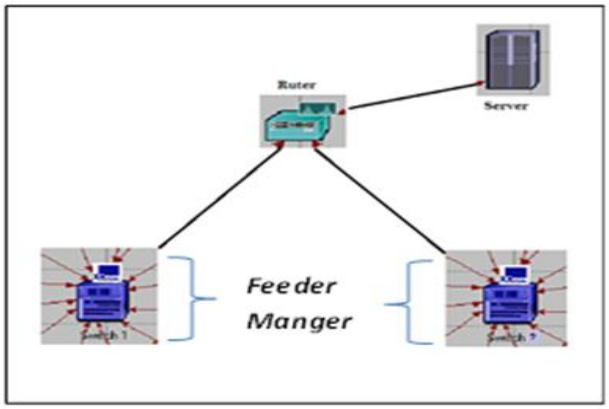
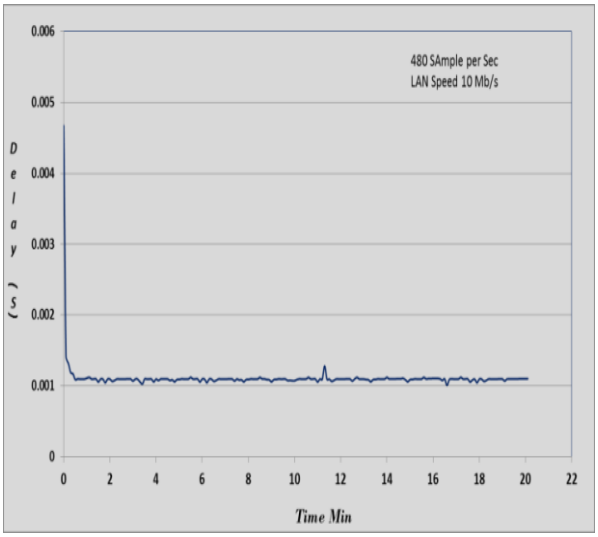


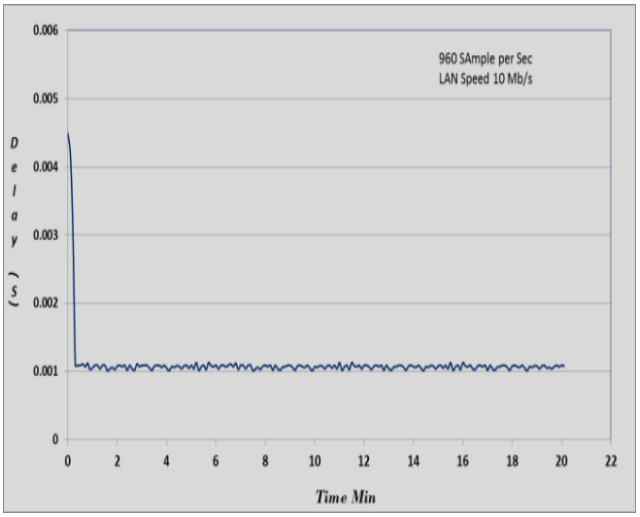
Figure.3. Shows two process bus in a star topology which are connected to router.

6.0 Simulation and Assessment

Different LAN speeds such as 10-Mb/s and 100-Mb/s was considered to observe the performance of GOOSE messages transfer in a star topology having multi-vendor IED's in a Feeder Manager (FM) of 33/11kV substation. The sample speed was also varied throughout the simulation to understand the response of SAS network of a typical star configuration and to evaluate the performance of the data transfer between IED's. It was observed that when the sampling rate was 1000 sample/s, it represented the worst case scenario having multiple file settings and data transfer files that were not so critical and could be low in priority for message transfer. However, when sampling rates were at 500 sample/s it represented tripping signals, which were given high priority within the protection system in a SAS network, these finding are exhibited in figures4 and 5



(a)



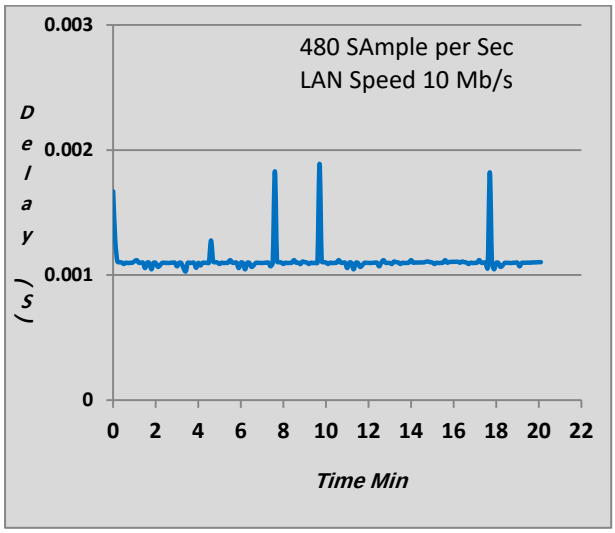
(b)

Figure. 4. (a-b): Delay in data transfer in **a Single** process bus at LAN speed 10Mb/s**.**

It shares a practical case for measuring delay time in exchanging Generic Object Oriented Substation Event (GOOSE) messages amongst the IED's. Further, it was observed that multiple vendor IEDs are flooding the LAN network with data packets and thereby slowing down the data transfer resulting in delay and compromising the protection.

Conclusion

With the development of DSAS and the application of IEC61850, Ethernet Network has



(a)

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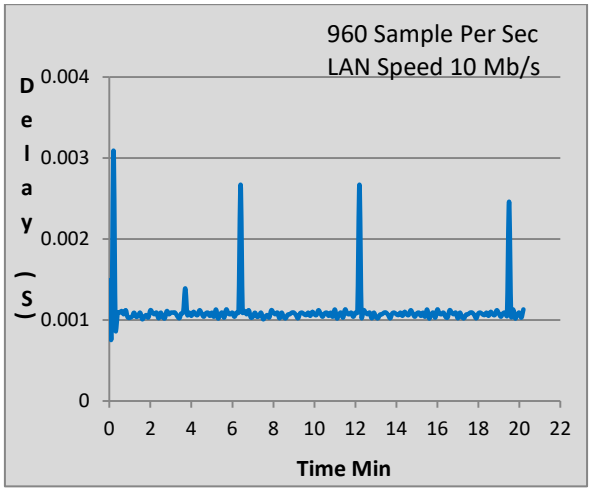

(b)

Figure. 5. (a,b): Delay in data transfer in **a double** process bus at LAN speed 10Mb/s**.**

become the main interconnection media in the DSAS. The performance of DSAS will be promoted if the performance of Ethernet Network is promoted. As the "bottle theory", the actual network performance relies on the node whose network performance is the worst, It addresses message transfer issues and delays including functional issues and redundancies. These simulations with different speeds and in different bus configuration provides the information for protection engineers, critical information with respect to protection reliability and interoperability of multi-vendor relays There are many factors that can impact

Ethernet Network. In the actual applications, the key factor should be found and disposed properly so that the network performance can be promoted obviously.

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